2. (Not Changed From Prior Version) The method according to claim 1, wherein the annealing is executed at a temperature lower than a melting point of single-crystal silicon.

3. (Not Changed From Prior Version) The method according to claim 1, wherein the annealing is executed at a temperature not less than 775°C.

4. (Not Changed From Prior Version) The method according to claim 1, wherein the annealing is executed at a temperature not less than 966°C .

5. (Not Changed From Prior Version) The method according to claim 1, wherein the annealing is executed at a temperature not less than 993°C.

6. (Not Changed From Prior Version) An SOI substrate manufactured using an annealing method of any one of claims 1.

7. (Not Changed From Prior Version) The substrate according to claim 6, wherein an HF defect density is not more than 0.05 defects /CM^2.

8. (Not Changed From Prior Version) A semiconductor device manufacturing method, comprising the steps of:

annealing an SOI substrate using an annealing method of any one of claims 1; and

forming an active region for a transistor in a nonporous semiconductor layer of the SOI substrate.

9. (Canceled)

10. (Not Changed From Prior Version) An annealing method of annealing an SOI substrate in a reducing atmosphere, comprising the step of:

holding the SOI substrate by a holding portion which contains no silicon carbide formed by sintering and has a surface formed from silicon carbide deposited by CVD and annealing the SOI substrate.

11. (Not Changed From Prior Version) The method according to claim 10, wherein the annealing is executed at a temperature lower than a melting point of single-crystal silicon.

12. (Not Changed From Prior Version) The method according to claim 10, wherein the annealing is executed at a temperature not less than 775°C.

13. (Not Changed From Prior Version) The method according to claim 10, wherein the annealing is executed at a temperature not less than 966°C.

14. (Not Changed From Prior Version) The method according to claim 10, wherein the annealing is executed at a temperature not less than 993°C .

15. (Not Changed From Prior Version) An SOI substrate manufactured using an annealing method of any one of claims 10.

16. (Not Changed From Prior Version) The substrate according to claim 15, wherein an HF defect density is not more than 0.05 defects /CM^2.

17. (Not Changed From Prior Version) A semiconductor device manufacturing method, comprising the steps of:

annealing an SOI substrate using an annealing method of any one of claims 10; and

forming an active region for a transistor in a nonporous semiconductor layer of the SOI substrate.

18. (Canceled)